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ms. B.4.6

to 0.45 times a length of a side of an opening in a pad provided on an active element surface of the semiconductor integrated circuit.

8. The piezoelectric device according to claim 1, wherein the base comprises a ceramic composite substrate.

5 9. The piezoelectric device according to claim 1, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is an Au bump.

10. The piezoelectric device according to claim 1, wherein a protrusion is formed in at least one side wall of the base facing the side of the semiconductor integrated circuit.

10 11. The piezoelectric device according to claim 10, wherein the protrusion is formed in each of side walls of the base facing two sides along the longitudinal direction of the semiconductor integrated circuit.

15 12. The piezoelectric device according to claim 10, wherein the protrusion formed in the side wall of the base has a substantially same height as, or is higher than, the semiconductor integrated circuit.

13. The piezoelectric device according to claim 10, wherein a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit is set to a range between 0.05 and 0.15 mm.

20 14. A piezoelectric device, comprising:  
a semiconductor integrated circuit; and  
a piezoelectric resonator element included in a package,  
wherein an opening is formed in the center of a base provided with an input/output electrode pattern, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the  
25 semiconductor integrated circuit is mounted in an opening, and the semiconductor integrated circuit is connected to an electrode pattern of the base through the plurality of bumps.

15. The piezoelectric device according to claim 14, wherein the plurality of bumps formed on the semiconductor integrated circuit are formed at regular

intervals at a center portion of the active element surface of the semiconductor integrated circuit.

16. The piezoelectric device according to claim 14, wherein a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

17. The piezoelectric device according to claim 16, wherein the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

18. The piezoelectric device according to claim 14, further comprising a layered part on which the piezoelectric resonator element is mounted and which surrounds the semiconductor integrated circuit, the layered part comprising at least two layers including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

19. The piezoelectric device according to claim 14, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

20. The piezoelectric device according to claim 14, wherein the base comprises a ceramic composite substrate.

21. The piezoelectric device according to claim 14, wherein the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

22. A piezoelectric device, comprising:  
a semiconductor integrated circuit; and  
a piezoelectric resonator element included in a package,  
wherein an opening is formed in the center of a base provided with an input/output electrode pattern, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in a center of an opening, and the

semiconductor integrated circuit is connected to an electrode pattern through the plurality of bumps by ultrasonic bonding means.

23. The piezoelectric device according to claim 22, wherein a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit is perpendicular to two opposing sides of the active element surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

24. The piezoelectric device according to claim 22, wherein a printing direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

25. The piezoelectric device according to claim 22, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

26. The piezoelectric device according to claim 25, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one being 80 to 90  $\mu\text{m}$  in diameter and 30 to 35  $\mu\text{m}$  in height, and the other being 40 to 45  $\mu\text{m}$  in diameter and 30 to 35  $\mu\text{m}$  in height.

27. The piezoelectric device according to claim 22, wherein the base comprises a ceramic composite substrate.

28. The piezoelectric device according to claim 22, wherein the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

29. The piezoelectric device according to claim 22, wherein a longitudinal direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

30. The piezoelectric device according to claim 22, comprising the semiconductor integrated circuit and the piezoelectric resonator element included in the package,

Year	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	

31. A method for manufacturing a piezoelectric device comprising a conductor integrated circuit and a piezoelectric resonator element included in a package, the method comprising:

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a step of hermetically sealing a metallic lid to the base.

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a step of hermetically sealing a metallic lid to the base.